Controllable Height of Regular Copper Array Using Electrochemical Plating

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Abstract: A novel bottom-up electrochemical plating technology is proposed and demonstrated. This reproducible plating technology possesses several advantages for fabricating regular copper arrays. The process eliminates surface voids and defects. Copper lines with 40 nm in width and copper pillar with 60 nm in diameter are formed by electrochemical copper plating combined with e-beam patterning. High quality crystalline copper lines and pillars were produced by making use of low electrolyte concentrations. Further, the height of structures was precisely monitored in situ by calculating the amount of charge needed for electroplating. This bottom-up plating approach meant that the over-fill problem commonly associated with electroplating could be avoided. The result was regular copper nanostructures. This technology could be applied in the manufacture of various nano-scale structures using different metals.

Key words: Copper, electrochemical plating, nanostructure.

1. Introduction

Nanoscale metallic lines have gained in importance in present-day integrated circuits. ECP (Electrochemical plating) is an easy, economical and high-throughput process for growing metallic lines and is commonly employed in semiconductor fabrication of copper lines. Since copper ECP can reliably fill nanoscale trench and hole arrays, it is used for copper interconnects in current technology nodes. Moreover, ECP technology has recently been applied to 3D ICs [1], in which vertically stacked chips are inter-connected using TSVs (Through-silicon vias) made by copper plating [2, 3]. However, the conductive seed layer used in the ECP process is grown by PVD (Physical vapor deposition) and may suffer from poor step coverage. More importantly, there is a risk of gap-fill pinch-off in the plating process due to plating rates at the bottom and sidewalls not being equal. This may result in unwanted voids in trenches and holes. A reliable plating technique utilizing a controlled plating rate for generation of void-free plated films with smooth surface morphology is highly desirable. Many methods for fabricating regular copper arrays, such as self-organized electro-deposition [4], AFM (Atomic force microscopy) tip lithography [5], template-assisted deposition [6] and electrodepositing into AAO (Anodic aluminum oxide) [7] have provided advances in copper-plating technologies. Here, we propose and test a novel approach offering controllable height in a bottom-up copper ECP process. In the process, copper structures are defined by a resist wall [8] and metallization height controlled to equal that of the wall. In this way, the high risk of voids commonly found in conformal plating technology is avoided. In addition, since only bottom-side plating is needed, there is no requirement for suppressor additives against side wall plating. This may help reduce impurities and hence increase crystallization in the copper array.

2. Experimental Methods

The copper-array pattern is defined by resist walls and holes. The process starts at deposition of the seed layer, which in this experiment is 60 nm-thick Au on top of a 10 nm-thick adhesion Ti layer. Both Au and Ti layers are made by thermal evaporation in a vacuum
chamber with a base pressure of $2 \times 10^{-7}$ mbar. Seed layers with conductivity higher than that of the target-plating layer are necessary for growth of a continuous metallic film, and a smooth seed layer is essential for high quality electro plating. Subsequently, regular arrays of ZEP520A resist wall sand holes are made by standard e-beam lithography using Elionix e-beam writer ELS-7500-EX. The resist is diluted so that the height of the walls can be adjusted to $60 \sim 100$ nm. The width of the walls is $25 \sim 40$ nm and the pitch of the array is two times of it. After development, the resist patterns are subjected to oxygen plasma cleaning for 30 s to remove organic residue at the surface of the seed layer. Brief ultrasonic cleaning and rinsing with deionized water keeps the bare seed surface hydrophilic, which is favored for good plating adhesion. The chips are then immersed into an electrolyte bath containing copper sulfate with 10% PEG 2000 (Polyethylene glycol 2000) and 10% sulfuric acid in deionized water (18 MΩ·cm$^{-1}$). Electroplating is driven at a constant voltage of $-0.4$ V at room temperature [9]. This voltage range is conducive to plating with crystalline copper growth. The polymer additives here play a major role in suppressing the plating rate during chemical reactions in order to improve the quality of copper crystallization. Sulfuric acid levels are adjusted to increase solution conductivity and prevent cathode voltage overflow. After this bottom-up ECP process, the resist isolator is dissolved using a dedicated organic remover ZDMAC (N, N-Dimethylacetamide) for several minutes. Then the chip is washed with deionized water to rinse off any remaining organic material and dried by nitrogen gas. Finally, the bottom-up copper lines and pillars are formed. As illustrated in Fig. 1, both copper lines and pillars can be fabricated. Line width and pillar diameter depend on the energy dosage of the resist during e-beam lithography.

3. Results and Discussion

Different electrolyte concentrations were tested during experimentation. A low concentration of CuSO$_4$ was used to supply sufficiently few ions inside the trenches and holes to suppress the plating rate during plating. Metallic electroplating is distinct from semiconductor electroplating due to differences in intrinsic characteristics such as components and conductivity. Studies using the alternating potential of reduction-oxidation reactions to make structures have previously been conducted. These include studies of single component copper [10] and hybrid multi-component CdSe [11]. However, in this experiment, a constant voltage is used during copper plating as it is necessary for creating highly regular copper arrays. It is found that the plating rate can be reduced to $2.5$ mm/s at an electrolyte concentration of between $10^{-4} \sim 10^{-6}$ M. The low plating rate provides advantages such as: 1) Good control of height to prevent over-fill of plating material; and 2) Improved uniformity and surface smoothness since there are fewer defects and voids after plating. The resist dense-pattern is made using an Elionix e-beam writer ELS-7500-EX at a dosage of $1.0$ μC·cm$^{-2}$. The lines are designed to be $10$ μm in length and serve as the standard for e-beam dosage testing. The resultant isolating resist walls formed exclude line collapse and line merges.

Fig. 2 is SEM (Scanning electron microscopy) images of plated copper lines and pillars made using the bottom-up ECP process, and Fig. 3 is cross-sectional TEM (Transmission electron microscopy) images of the dense lines corresponding to Fig. 2a. The structures were plated using an electrolyte concentration of $6 \times 10^{-6}$ M. Fig. 3a indicates that the height of plated

![Fig. 1 Diagrams of the arrays of copper (a) lines and (b) pillars. The resist isolator is removed after copper plating.](image)
copper lines is the same as that of the resist. In this case, under the given electrolyte concentration, copper height is dependent on plating time. The total volume of strictly regular copper structures achieved is 3,500 μm³. This includes lines, pillars and remark patterns. By ionic charge calculation during reactions, the total weight of copper ions distributed among the patterns is close to $3 \times 10^8$ g.

Fig. 4 shows the plating current as a function of time and current ratio for the copper plating lines depicted in Fig. 3. Initially current is high but soon displays exponential decay. After about 5 s, the curves indicate near saturation occurring. Copper conductivity shows to be intrinsically less than that of the gold seed layer.

As plating occurs, this is directly revealed in the current decay. In this report, initially total charge integrated over time is used, as this value agrees well with the results of plating volume. This helps control well the height of metallization. From the black curve in Fig. 4a, it is found that the total amount of charge integrated over the area of current with time involved in the plating is $4.06 \times 10^4$ C. Total charge corresponds well with the amount of copper plating estimated for the trench and holes. In this calculation, we use a copper reduction reaction formula $\text{Cu}^{2+} + 2e^- \rightarrow \text{Cu}$ to form copper plating at the cathode electrode. This calculation allows for precise determination of plating time as well as the height of
plated structures. Height uniformity of the plated array can be determined using Fig. 3b. It is found that structures along edges are slightly higher due to non-uniformity in plating current distribution in the electrolyte. This uniformity problem is more serious for high concentration electrolytes. This can be clearly seen in the lines and pillars plated using an electrolyte concentration of $1.0 \times 10^{-4}$ M shown as the curve in Fig. 4a. An average ratio of about $4.6 \pm 0.5$ for plating current between high and low electrolyte concentrations is shown in Fig. 4b. It is interesting to note that although concentration differs by 16.7 times, current for high concentration is only about 5 times higher. Also, there is a constant variation in the difference of the value of current divided by concentration. Finally, current ratio increases with time. This may be attributed to the local “depletion” of electrolyte ions in the vicinity of structures, especially in low concentration cases. These results all indicate that plating height can be well-controlled by concentration and current.

Fig. 5 shows TEM images of the interface between plated copper and gold. Fig. 5a shows the different layers that form the substrate and gold’s interface with copper. Fig. 5b is a close up of the gold-copper interface. The use of oxygen plasma cleaning of the gold surface before plating meant that all organic residues were removed so that once plating was completed the interface between gold and copper reflected single crystalline Cu/Au structures without lattice mismatching. Fig. 5b shows that the plated copper has a crystalline grain structure with a lattice constant of 2.43 Å. The lattice image also reveal show clean the interface between copper and gold is and a remarkable lack of defects and voids.

Fig. 6 shows the spectrum of Cu2p binding energy observed by XPS (X-ray photoelectron spectroscopy) [12]. The peaks of XPS spectra in Fig. 6 are the binding energy of Cu2p3/2 and Cu2p1/2 located at 932 eV and 952 eV respectively. The results indicate the
4. Conclusions

Bottom-up ECP plating technology for producing regular copper structures is demonstrated. Plating electrolyte concentration was optimized at approximately $6 \times 10^{-6}$ M, and plating rate at 2.5 nm/s. Using a low plating rate, the height of the structure can be precisely controlled to match that of the resist, and thus prevent copper over-fill. The crystalline plated structures are found to be free from defects and voids. This can prevent the over-fill problems encountered when plating dense pattern sand also reduce total copper usage. Furthermore, removal of the resist after plating is simpler than that of low-k dielectric used in conformal plating. This method demonstrates a novel metallization approach to high-purity highly regular copper nanostructures.

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References