Cascaded H-Bridges Asymmetrical 11-Levels Optimization

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Abstract: The following dissertation aims at investigating the multilevel topology basis through the analyses of the harmonic elimination control modeling methodology of the asymmetrical inverter. Thus the contribution of this paper can be summarized mainly by the fact that the pre-calculated PWM control used to control the symmetrical structure, as applied to the asymmetrical structure with a reduced number of cells, provides the same performance level resolution and signal strength to the load terminals, which guarantees a constant voltage frequency report. This observation is similar for the three cells, which allows the use of different drivers such as MOSFET, IGBT and GTO. These results have a good performance from the intrinsic proprieties of each semiconductor for each cell.

Key words: Cascaded H-bridge asymmetrical converters, harmonic elimination control, THD.

1. Introduction

Cascade multilevel inverter (CMLI) is the more recent and popular type of electronic converter power that synthesizes a desired output voltage from several dc voltages levels as inputs. It can be synthesized a nearly sinusoidal voltage waveform when sufficient number of dc sources is available. CMLI offers several advantages such as, its capabilities to operate at high voltage with lower dv/dt per switching, high efficiency and low electromagnetic interference (EMI). It is considered as one of the most important topology in the family of multilevel and multi pulse inverters. It requires least number of components when compared to diode-clamped and flying capacitors type multilevel inverters and contrary to multi pulse inverter there is no need for a special designed transformer. It has modular structure with simple switching strategy and occupies less space [1-3].

A complete analysis for an 11-levels inverter using 5 H-bridges per phase then 3 H-bridges in series is

presented. The focus is on a general design principle of a uniform step 11 levels converters; with K series-connected full bridges inverters per phase. A new design terminology is proposed and analytical relationships are established. Simulation results shown the reliability of the design approach suggested.

2. Survey of Cascaded H-Bridge Asymmetrical Topologies

2.1 Cascaded H-Bridge Multi-levels Concept

To overcome the limitations related to the maximum capacity blocking voltage of the existing semiconductor devices power and to provide a large number of output levels without increasing the number of converters, asymmetrical 11-levels converters (A11LC) can be used [3, 4]. The investigated topology is presented in Fig. 1 with 5 symmetrical cells [(a)] and 3 asymmetrical cells [(b)] cascaded H-bridge legs.

Fig. 1 lets understand the operating principle of the modules composing the leg of a generic n-levels converter. In this kind of multi-levels converter, all the possible cell output levels are exploited. While there

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Fig. 1 Configuration of single-phase series H-bridges 11-levels generated by: a) 5 symmetrical cells - (b) 3 asymmetrical cells.

are no limitations on the level of diode-clamped or flying-capacitor inverter, which can be even or odd, cascaded H-bridge can have only odd numbers of levels; since the first cell provides three levels whereas the others always add two levels more. So Fig. 1 permits to put symmetrical versus asymmetrical multi levels converter (AMLC).

As shown in Fig. 1a, the SMLC is defined by the fact that all feeding partial DC-voltages sources (DCVS) are equivalent, have the same value and are series connected. In practice there are no such limits, and hence the DCVS can be different. The DCVS are proposed at Fig. 1b to be chosen according to a geometric progression with a factor of 2. Fig. 1b proposes to use GTO switches for the large cell and IGBT switches for the small one. This latter solution is known as AMLC. It is worth mentioning that choosing the same input voltage (Fig. 1a) for each inverter allows obtaining the maximum output voltage with the minimum number of cells and given switches. Whereas choosing different input voltages (Fig. 1b) for each cell allows obtaining the maximum output resolution with the minimum number of cells. This distinction clearly shows two different fields of applications, high voltage inverters and high resolution inverters, which correspond respectively to symmetrical and

asymmetrical multi levels inverters. Certainly, if a higher resolution for a high voltage inverter is needed, it is possible to combine the two techniques.

2.2 Multi-levels Cascaded H-Bridge Asymmetrical Inverter Performance

Asymmetric multi levels converters (AMC) can optimize the number of output levels (any odd number from $2K + 1$ to $3K$), by using H-bridges scaled in power of three, without increasing the number of converters. Indeed it is true that "Asymmetrical" topology has the advantage of providing more flexibility of the designer, yet its shortcoming cannot be denied as the H-bridges are not interchangeable and therefore under certain faulty conditions, the converter cannot operate.

The AMC go one step further through the variation of DCVS in binary fashion, which gives an exponential increase in the number of levels. For 'n' such cascaded inverters, with DC voltage levels varying in binary fashion, $2n + 1$ distinct voltage levels may be achieved. The DCVS supplying partial inverters are supposed to be rationally unbalanced.

AMC are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, they present several

other advantages. First of all, they generate better output waveforms with a lower dv/dt than the standard converters. Then AMC increase the power quality due to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses. Furthermore, AMC can operate with a lower switching frequency than 2-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Besides AMC can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

3. H-Bridge Asymmetrical 11-Levels Optimization

In general, the Fourier series expansion of the staircase output voltage waveform is as shown in Fig. 2.

A reference function is quantified by a discrete voltage waveform with a finite (11) number of steps. The possible output voltages of the converter are V_{A5} , V_{A4} ... V_{A1} . An output voltage step is defined by the difference between two consecutive voltages.

In order to put symmetrical versus asymmetrical multi levels converter (AMLC), harmonic elimination control will be first analyzed and applied to both them. Then the control strategy will be presented and applied for both SMLC and AMLC, too. Finally asymmetrical 11-levels optimization will be conjured up.

3.1 Harmonic Elimination Method

In applications where the voltage magnitude and the frequency are relatively fixed, we are not in need of a modulated voltage [4]. In this case, the fundamental wave is sufficient for the voltage generation whose

harmonic rate of distortion is weak. The harmonic elimination method consists in quantifying this reference voltage, in a given number of steps [5].

This technical modulation will be used to control symmetric multilevel inverter with five series-connected H-bridges. It consists in obtaining the output voltage of the inverter formed by a succession of variable widths crenels [5]. Generally, a wave that has a double symmetry compared to the quarter and the half-period is used. This wave is characterized by the number C of crenels or impulses by alternation. Whether odd or even number, C also represents the number of angles of overlap per quarter of period and determines the width of the whole of the crenels. The angles of overlap are given in such way to eliminate certain harmonics. In the present study we were interested to eliminate the first harmonics (5, 7, 11, and 13). Fig. 3 illustrates the waveforms and switching method of 11 levels cascade inverter.

The magnitude of the AC output phase voltage is given by

$$V_{AN} = V_{A1} + V_{A2} + V_{A3} + V_{A4} + V_{A5}$$

In general, the Fourier series expansion of the staircase output voltage waveform as shown in Fig. 2. The output waveforms have a double symmetry compared to the quarter and the half-period thus the angles of condition must satisfy the following condition:

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \frac{\pi}{2}$$

The output voltage V_{AN} is given by the voltage steps waveforms such as the one depicted in Fig. 3 with 5 steps, the Fourier transform for this waveform is as follows:

Fig. 2 Staircase output voltage waveforms V_{A1} for first cell.

Fig. 3 Wave forms and switching of 11 Levels Cascade inverter.

$$V_{AN}(wt) = \frac{4E}{\pi} \times \sum [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)] \times \frac{\sin(nwt)}{n} \quad (1)$$

where $n = 1, 3, 5, 7, \dots$

From Eq. (1), the magnitude of the Fourier coefficients when normalized with respect to E is as follows:

$$H(n) = \frac{4}{n\pi} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)] \quad (2)$$

The modulation index m_a is defined by:

$$m_a = \frac{V_{AN}^*}{V_{AN,max}} \quad (3)$$

V_{AN}^* : Magnitude of output voltage desired.

$V_{AN,max}$: Maximum magnitude of inverter = $5E$.

3.2 Control Strategy

The five switching angles, θ_i ($i = 1, 2, 3, 4$ and 5), are calculated offline to minimize the harmonics for each modulation index m_a in order to have a total output

voltage with a harmonic minimal distortion rate. The correct solution to Eq. (5) leads to the fact that the output voltage of the 11-levels inverter will not contain the 5th, 7th, 11th and 13th harmonic components.

$$\begin{aligned} \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) &= 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) &= 0 \\ \cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) &= 0 \\ \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) &= 5m_a \end{aligned} \quad (5)$$

The evolution of conduction angles is according to the modulation index m_a such as it depicted in Fig. 4.

For a better optimization of the waveform of the output voltage and for a modulation index $m_a = 0.9$, the conduction angles are as follows:

$$\begin{aligned} \theta_1 &= 5.5510^\circ, \theta_2 = 16.3669^\circ, \\ \theta_3 &= 23.2811^\circ, \theta_4 = 38.2607^\circ, \theta_5 = 58.699^\circ \end{aligned}$$

The angles θ_i , ($i = 1, 2, 3, 4$ and 5) are used to start the switches, the control signals equivalent to these angles are shown in Fig. 5.

This strategy of control based on the conduction angles choices which satisfy the condition of symmetry,

Fig. 4 Evolution of conduction angles according to modulation index.

allows us indeed to have the commutation frequency of the switches equal to the fundamental frequency one, which minimizes the commutation losses. Yet different cells don't have the same conduction time, which results in an unbalance in the distribution of the conduction losses.

It can be seen from Figs. 6 and 7 that:

- With a symmetrical supply we obtain an output voltage that has $2 \times 5 + 1$ levels of output voltage peak to peak;
- The output voltage has a good harmonic distortion

rate (THD_v = 8.33%) with harmonics elimination (5, 7, 11, 13).

3.3 H-bridge Asymmetrical 11-Levels Optimization

To achieve the same performance as the topology of Fig. 1a SMLC characterized by DCVS identical and isolated, consisting of 5 cells with identical switches, and voltage AC output per phase V_{AN} 11 levels; we opt for the asymmetrical topology H-bridge having a reduced number of cells (3 instead of 5) in Fig. 8. We note that:

Fig. 5 Different control signals for all cells [1-6].

Fig. 6 Wave form voltage of symmetrical multilevel inverter with five series-connected H-bridges by elimination harmonic method.

Fig. 7 Harmonic rates of the output voltage.

Fig. 8 Series 3 asymmetrical cells.

Fig. 9 Staircase output voltage waveform for 3 asymmetrical cells.

$$V_{A1\max} = E, V_{A2\max} = 2.E, V_{A3\max} = 4.E$$

- The DCVSs of each cell are chosen in a way that enables to have a well determined run level of VAN 11 levels as shown in Fig. 9;
- For each cell we use identical switches having the same technical parameters, but different from switches of the two others cells. Indeed voltage caliber and size of switches of each cell must be superior and higher than the corresponding DCVS: ($V_{Ti.1} > E$, $V_{Ti.2} > 2E$, $V_{Ti.2} > 4E$).

4. Simulation and Results

We use the same angles θ_i $i = [1, 2, 3, 4 \text{ and } 5]$ point out before.

The signal control and the output voltage of each cell relative to the angles are logging at Fig. 10. So we note that:

- The total number of each cell commutations depends on the value of the voltage which feeds it and therefore on its position in the structure of the converter.

- More the supply voltage of a cell is grand with regard to the others less those switches commuted.

The output voltage and the THD are given respectively by Figs. 11 and 12.

The 3 series cells AMLC the DCVS respectively E , $2E$, $4E$ represent a supplementary degree of liberty which consist and permit to generate output phase voltage V_{AN} 11 levels having the same $THD_v = 8.33\%$ with a reduce cells number (3 cells).

Table 1 shows the result before and after the optimization using the asymmetrical topology. This strategy obtains the same value of THD_v (8.33%) using

Fig. 10 Different control signals and output voltages.

Fig. 11 Wave form voltage of asymmetrical multilevel inverter with three series-connected H-bridges by elimination harmonic method.

Fig. 12 Harmonic rates of the output voltage.

Table 1 Asymmetrical 11-levels optimization.

Topology	Cells number	Semiconductors number	THD _v
Symmetrical	5	20	8.33%
Asymmetrical	3	12	8.33%

only 3 cells and 12 semiconductors.

5. Conclusions

This paper deals with asymmetrical multi-levels inverters. A generalized design principle of an asymmetrical multi-levels converter is presented. The investigated topology is based on K series-connected full bridges inverters per phase. It consists of series connected cells with different input voltages.

A complete analysis for 11-levels inverter has been presented and has shown that a significant amount of

THD reduction can be attained if all possible solution sets are computed. It has been shown that there are many possibilities to feed the partial H-bridge inverters to enhance the number of output voltage levels, without increasing the number of power switches [1, 4]. The cascade H-bridge asymmetrical 11-levels optimization is based on the choosing of different input voltages for each cell. This allows obtaining the maximum output resolution with the minimum number of cells.

This distinction clearly shows two different fields of applications, high voltage inverters and high resolution inverters, which correspond respectively to symmetrical and asymmetrical multi-levels inverters.

A new optimal switching control strategy for these latter inverters is proposed. This strategy obtains the optimal result in terms of harmonic rates of the output voltage and consequently in terms of switching losses.

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