Journal of Materials Science and Engineering B 5 (1-2) (2015) 1-11
doi: 10.17265/2161-6221/2015.1-2.001

A Study of the Thermal Characteristics of NiCuZn Ferrite Chip Inductors

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Abstract: Like other electrical components, the characteristics of magnetic components are significantly affected by not only magnetic fields, but also ambient temperature and inner/outer stress. In order to understand the nature of inductance shift of NiCuZn ferrite after thermal treatments, in this work we measured and analyzed the inductance shift of inductors which were treated separately by reflow and temperature cycling conditions. The results reveal that the inductance shift comes from not only residual stress release, which causes an increase in inductance during the cooling stage, but also the change in magnetic status by the peak temperature, which also causes an increase in inductance. Nevertheless, this magnetic status would be affected by the magnetic field to form a remanence that causes a fall in inductance later on, and this remanence level can be reduced under subzero temperature conditions. Comparing the construction of components for multilayer chips made of pure ferrite with those made of wound coil, this complex relation between heat, stress and the magnetic field of chip inductors are caused by the cofiring of ferrite and conductor material during the manufacturing process of chip inductors.

Key words: Thermal treatment, stress, cofiring.

1. Introduction

Due to the nature of magnetic materials, especially in NiCuZn ferrites, components made of such materials are sensitive to temperature, and even the heat during the soldering process and temperature changes from the local climate during use can affect the inductance level of components. However, we can use two treatment conditions and apply them to components to learn their temperature characteristics in these two situations. The first treatment condition is called reflow, which simulates the process of soldering, the second one is called TC (temperature cycling), which simulates the extreme temperature conditions that may be encountered during use.

One of the factors that causes inductance is permeability, which has three majors parameters, which are the saturation of magnetization, *MS*, the first order anisotropy constant, *K1*, and the magnetostriction constant, λ. *MS* and *K1* are sensitive to temperature, and the ratio of $\lambda/K1$ reflects the material's sensitivity to stress. Because *K1* affects both the temperature and stress characteristics of ferrite materials, these characteristics might interact. *MS* contains two parts, which are the spin rotation and domain wall motion, and the literatures [1, 2] mention that the former is sensitive to temperature while the latter is not. Therefore, if the spin rotation contributes more permeability than the domain wall motion does, the inductance of components will be more sensitive to temperature. On the other hand, the literature also states that, because the domain wall motion is related to the microstructure of components, its contribution to permeability can be increased by increasing grain size and reducing the porosity inside the grains, as this can reduce the effect of spin rotation, and thus the temperature sensitivity of the component will be

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reduced. In contrast, with regard to spin rotation, *K1* and λ have a close relation with the chemical composition of ferrite materials [3-5], although some studies [6, 7] find that these factors can be adjusted under 600 ^{o}C ~ 1200 ^{o}C heat treatment, which changes the distribution of cations in the A and B sites of the spinel.

The soldering process and ambient temperature often affect the inductance of inductors. While the ambient temperature range is generally between -10 ^{o}C ~ 260 ^{o}C, very few studies focus on the performance of chip inductors at these temperatures. This work focuses on chip inductors made of NiCuZn ferrite and their performance between -40 ^{o}C ~ 300 ^{o}C. We applied the reflow and TC thermal conditions to the samples, and analyzed its inductance response during each part of the TC profile to uncover the contribution of each stage of the thermal treatment profile to the inductance shift.

2. Experimental Setup

2.1 Sample Preparation

2.1.1 Chip Type Samples

We used the formula powder (with the composition shown in Table 1) to prepare slip and foil, and printed the silver paste for 8.5 turns as a coil on the foils, then stacked, laminated and cut it into a chip with the dimensions of 2.5(l) × 2.0(w) × 1.0(t) mm, then fired the samples at 870 ^{o}C for 60 min, dipped the termination paste on the end of the component, cured the termination at 700 ^{o}C for 40 min and plated it to complete the chip sample preparation process.

2.1.2 Circular Type Samples

The NiCuZn ferrite foils prepared in step 2.1.1 were stacked to make circular type samples of 1.0 mm thick and with inside and outside diameters of 7 mm and 17 mm, respectively, and these then underwent uniaxial pressing with 2000 psi of pressure. The samples were then fired at 870 ^{o}C for 1 h. After firing, copper wires were wound around the samples 14 turns each for the primary and second windings as coils, respectively.

Table 1 The composition of the chip type and circular type samples.

Composition	Fe_2O_3	NiO	CuO	ZnO
Mol%	48.3	15.3	9.7	26.7

2.2 Treatments and Measurements

2.2.1 Chip Type Samples

Two treatments were used in this work, reflow and TC. The reflow treatment was carried out with a peak temperature of 270 ^{o}C and 3 min of soak time. The TC temperature ranged from 125 ^{o}C ~ -40 ^{o}C, with 30 min of soak time for 125 ^{o}C and -40 ^{o}C, and the temperature change in 5 min interactively. 1A of current bias test was applied to the components. All the inductance values had to be changed to percentages, for which the nominal value was 4.7 μH, in order to calculate the rate of change. The treatments are described below, and all the components were sintered at 870 ^{o}C, unless otherwise stated.

(1) After the treatments, a current bias was applied to components in order to measure the inductance and analyze the inductance distribution in each stage of the process.

(2) The same treatment was carried out twice for first set (Reflow + Reflow and TC + TC), while two different treatments were carried out for the second set (Reflow + TC), and a test similar to the second set was then carried out for the third set, with the treatment sequence reversed (TC + Reflow).

(3) Some components prepared by section 2.1.1 were sintered at 895 ^{o}C and step (1) was performed.

(4) The L-I (inductance-current) characteristic was measured when the current was 0A to 1A to 0A.

(5) Heat treatment was performed for 3 min with different peak temperatures, and then the inductance of the first set was measured, and the inductance with rising temperature was also measured in real-time.

(6) Heat treatment was performed at 270 ^{o}C with different soak times.

(7) Cooling from the different peak temperatures were carried out by immersing the components in

water.

(8) Different cycles, peak temperatures, and lowest temperatures were used for the temperature cycling treatments.

2.2.2 Circular Type Samples

The samples prepared in step 2.1.2 underwent the TC treatment (125 ^{o}C ~ -55 ^{o}C for 30 min, 40 cycles), and reflow treatment (270 ^{o}C for 3 min), and then the maximum flux density (*Bm*) and maximum remanence (*Br*) for each current level were measured (IWATSU-SY8258).

2.3 TMA for the ferrite sample.

Using TMA (thermomechanical analysis) to analyse the ferrite samples.

3. Experimental Results

Comparing the inductance level before and after thermal treatment for the chip samples, as shown in Fig. 1, the "reflow treatment" saw an 11% rise in inductance; however, when the same thermal treatment was performed again, the increase in inductance was only 0.68%. The same phenomenon was also observed for the "TC treatment," in which the shifts in inductance were 5.9% and -1.9% for first and second TC treatments, respectively. Both of these thermal treatments showed minor differences in inductance in the second treatment, and this reveals that preliminary thermal treatment is an effective way to reduce sensitivity to temperature and make components more stable during soldering or in drastic changes in ambient temperature. We also observed the inductance distribution before and after thermal treatments for the chip samples, and the results are shown in Fig. 2. It shows that both of these treatments drove the whole all the inductance values to move left and narrow the distribution. We ordered the data from small to large values, and separated the first half as the small-value set (D1 ~ D50, 1.36% in average) and the second as the large-value set (D51 ~ D100, 13.2% in average) to further analyze the data, and the results are shown in Table 2. By analyzing the change in inductance distribution before and after the treatments, it can be seen that the level of the rise in inductance is related to the initial inductance. In other words, the small-inductance group saw a relative bigger rise in inductance, and the large-inductance group had a

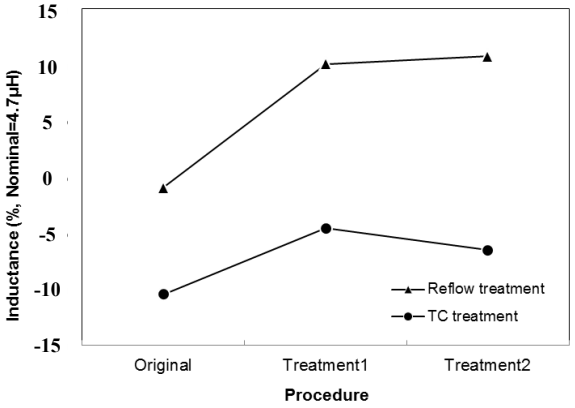
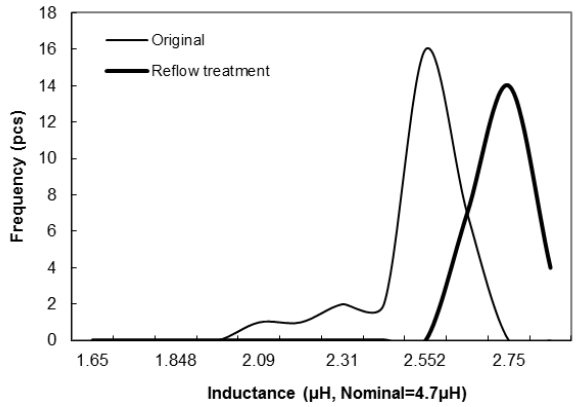
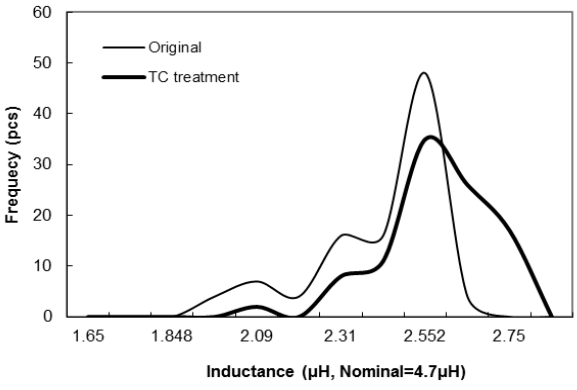


Fig. 1 The inductance shift of chip samples after two treatments in series.



(a)



(b)

Fig. 2 The inductance distribution of chip samples before and after treatments, (a) reflow treatment, and (b) TC treatment.

Table 2 The increase in inductance of the lower and higher inductance groups of the chip samples after reflow and TC treatments.

Original inductance	Inductance change after reflow treatment (%)	Inductance change after TC treatment (%)
D1 ~ D50	11.87	10.2
D51 ~ D100	8.33	4.2

relatively smaller one, and this explains why the distribution of the inductance values is clustered in Fig. 2. Furthermore, the TC leads to more a significant difference in the increase between the small-inductance and large-inductance groups comparing to the reflow treatment, while the reflow lead to a greater increase in inductance than the TC did.

We prepared other chip samples sintered at 895 °C and performed the same reflow and TC treatments. The results are shown in Fig. 3, and it can be seen that when the sintering temperature was raised from 870 °C to 895 °C, the rise in inductance increased from 6% ~ 11% to 35% ~ 40%, meaning that the sensitivity to the temperature increased significantly. As we know from the literature [1], the grain size increases and porosity inside the grains reduces when sintering temperature is increased, and this promotes domain wall motion, which reduced the temperature sensitivity of inductance of components. However, our results showed the opposite process. TMA treatment of ferrite material was performed, and the results are shown in Fig. 4, and it can be seen that the shrinkage of the ferrite further increased as the sintering temperature rose higher, and this leads to a greater stress inside the components, and so we can conjecture that more residual stress might have been released by the thermal treatment, thus causing the greater rise in inductance. In other words, different sintering temperatures would create different kinds and levels of stress inside the components, and once the components heat up, this stress would be released, leading to a rise in inductance. The literature [9] mentions that most kinds of stress, including compression and tension, reduce permeability, and combined with the shift in the distribution of inductance shown in Fig. 2, the chip samples with lower inductance might have higher residual stress, which was then released when exposed to greater heat, causing the greater increase in inductance.

Magnetic components have a higher sensitivity to temperature, stress and the magnetic field created by current bias. We applied 1A of current bias to the chip samples which had undergone reflow and TC treatment, and then observed the shift in inductance. The results are shown in Fig. 5, which reveals that the inductance of the samples that underwent TC treatment remained almost constant, while those underwent reflow treatment saw a dramatic fall in inductance, and this drop was directly proportional to bias level. Based on this result, it can be supposed that the bias would counteract the increase in inductance of components which had undergone reflow treatment. It is known that current bias will create a magnetic field inside the components. Therefore, the increased inductance which could be counteracted by this bias must be sensitive to the magnetic field, that is, some of the increase

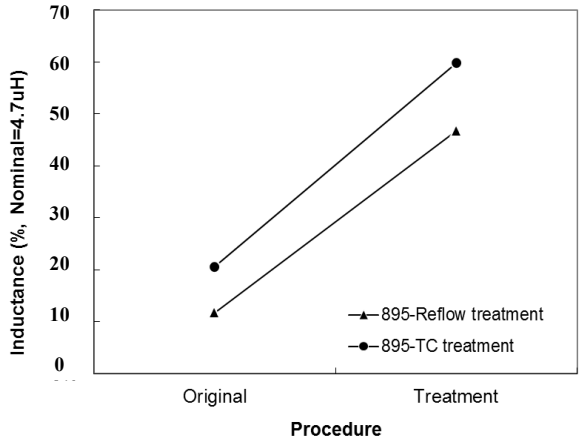


Fig. 3 The inductance shift of chip samples firing at 895 °C.

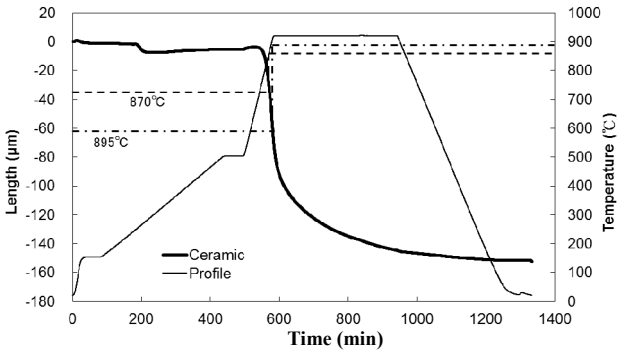


Fig. 4 The TMA of NiCuZn ferrite material.

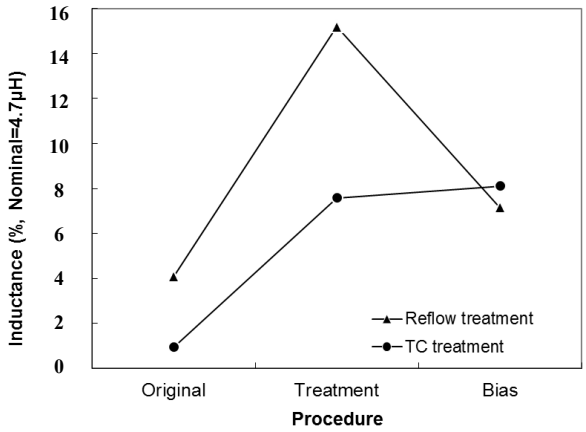


Fig. 5 The inductance shift of chip samples after bias for each treatment.

in inductance after reflow might come from the change in magnetic status. Some studies [6, 7] apply treatment temperatures as high as 600 °C ~ 1200 °C, which is high enough to drive the ions to a new site of the spinel. However, the treatment temperature in this work was lower than 300 °C, and there was thus not enough energy to cause redistribution of the ions.

We also prepared circular samples made of pure ferrite material to study the reflow and TC treatments individually to compare their performance with that of the chip samples. Their B-H (flux density – magnetic field strength) curves are shown in Fig. 6(a), and both the maximum of flux density (*Bm*) and remanence (*Br*) for each current level are consistent with their B-H features when the circular samples underwent reflow or TC treatments. On the other hand, Fig. 6(b) shows the L-I (inductance-current) curves of chip samples after reflow and TC treatments, and their features are very different. The "TC sample" had the same initial and final inductance when the current returned back to 0A, whereas the final inductance level was smaller than the initial one for the "reflow sample". This reveals that the chip samples could have remanence after bias if they had first undergone the reflow treatment. That is, the counteraction of increase in inductance of the chip samples was caused by remanence, which was induced by the interaction between the change in magnetic status and the magnetic field from the current bias. The literatures [7, 11, 12] mention that the remanence relates to magnetostriction and anisotropy constants, and they can be altered by a very high temperature treatment. Heating is one way to demagnetize materials, as heat can force the spin rotation and domain wall motion to return to a disordered status, and the components in this stage could have a very high inductance level, as the greatest amplitude of spin rotation and domain wall motion would be obtained. Nevertheless, the increase in inductance coming from spin rotation and domain wall motion is sensitive to the magnetic field, and thus the higher the magnetic field, the higher the remanence will be after thermal treatment, causing a greater fall in inductance. With regard to the components that underwent TC treatment, none of the increases in inductance were affected by the bias, and this reveals that these increases all came

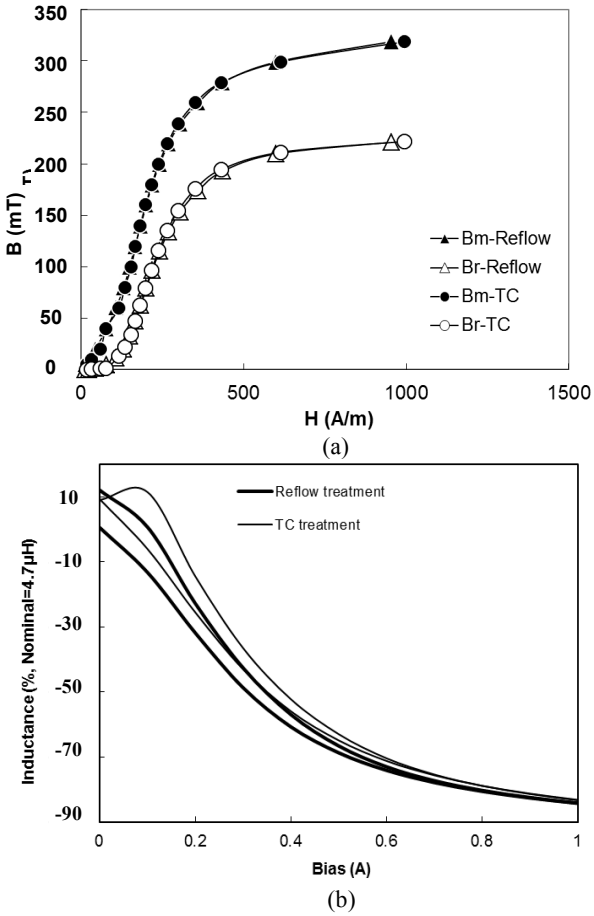


Fig. 6 (a) The maximum flux density (*Bm*) and maximum remanence (*Br*) of before- and after-treatment of circular type samples; (b) the L-I curve of before- and after-treatment of chip type samples.

from the release in stress instead of the change in magnetic status, and also that there might be one condition of the TC profile that could inhibit the remanence after the bias.

We then applied different thermal treatments to the components continuously, and then repeated this using the opposite sequence of treatments for other components, and the results after bias are shown in Fig. 7. As shown in the earlier results, the inductance would no longer change if we applied the same treatment twice to a chip sample, but it would change, and do so in a different way, if we applied two different treatments in series and changed their order. For the set of Reflow-TC, there was a difference of around 8% compared to the original inductance level after bias, while for the set of TC-Reflow, the difference was almost 0%, which was far more than the increase in inductance coming from the reflow or TC treatments. This reveals again that the source of the increase in inductance from the reflow and TC treatments was different. Reflow + bias will causes a drastic drop in inductance, but TC + bias does not. However, Fig. 7 shows that no matter where in the treatment sequence TC occurs, the fall for both sequences is greater than the increase after TC treatment. Because the increase in inductance with TC treatment comes only from the stress release and is irreversible, this means that the residual stress will not be released again. That is, the result shows that the level of change of the magnetic status would increase after the residual stress is released. The literature notes that residual stress inhibits magnetization [4, 10], and thus when the residual stress is released, the level of change in the magnetic status caused by heat will then increase.

The results outlined above show that even though both reflow and TC are thermal treatments, they are very different with regard to the remanence. To understand the effects of each part of the TC profile on the inductance, we analyzed the whole TC profile and separated it into the peak temperature level, soak time, cooling rate, cycling and subzero temperature. Fig. 8 shows the results for each peak temperature level of treatment, and shows that the inductance rose as the temperature increased, and reached the maximum value at around 250 ^{o}C ~ 270 ^{o}C, after which it started to fall. Fig. 9 shows the temperature characteristics of the sample, and it can be seen that, the Curie point of chip sample is around 250 ^{o}C. Comparing Figs. 8 and 9, the peak treatment temperature around the Curie point coincided with the maximum increase in inductance. Based on this result, we used 270 ^{o}C as the treatment temperature and with different soaking times for the chip samples, and the results are shown in Fig. 10. It can be seen that the increase in inductance rose before 30 min and then, surprisingly, as the time increased further, the increase in inductance then began to fall. Because the shift in inductance shift comes from the changing of two statuses inside the components, which are the stress and magnetization, so the rise and fall in

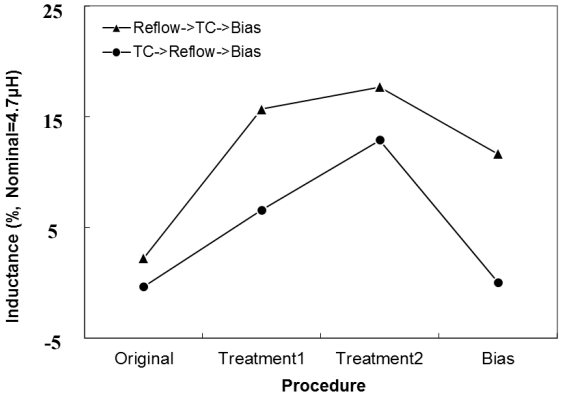


Fig. 7 The inductance shift of chip samples after two different thermal treatments in series.

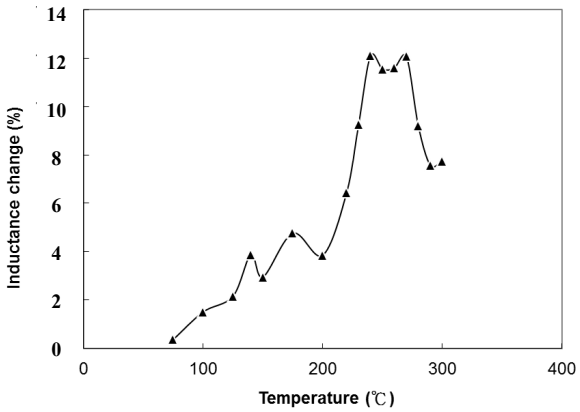


Fig. 8 The inductance shift of chip samples after thermal treatment with different peak temperatures.

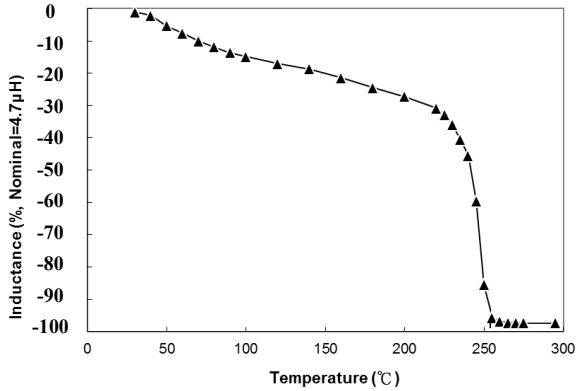


Fig. 9 The temperature characteristic of the inductance trend of chip samples.

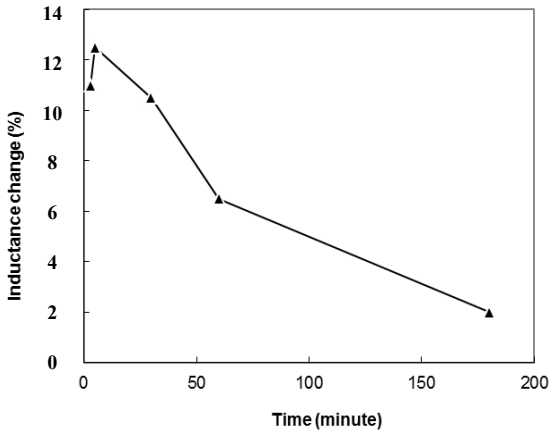


Fig. 10 The level of inductance of chip samples treated at 270 °C with different soaking times.

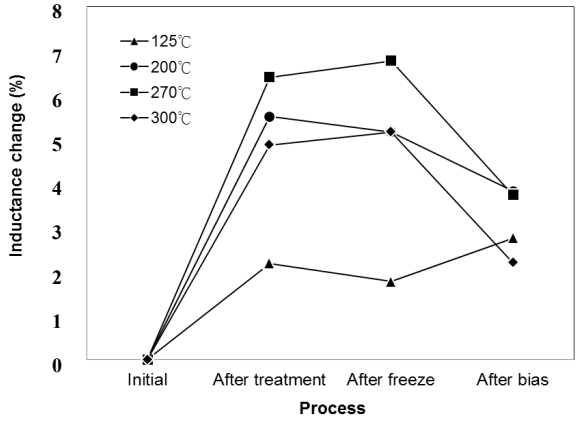


Fig. 11 The inductance shift trend of chip samples which were cooled from different peak temperatures.

inductance should be connected to the changes in these two factors.

For the next experiment, we pre-heated the chip samples to different peak temperatures and cooled them in water to simulate the temperature shift stage in the TC profile. The results are shown in Fig. 11, and it can be seen that when the peak temperature increased, the increase in inductance also rose and reached the maximum value at the temperature of 270 °C. However, compared with the results of normal TC treatment, all the increases in inductance in this experiment were only half as large. As stated in some studies [6, 7], when the cooling rate is high enough, it can freeze the ion status produced at high temperatures, and this will result in a low level of anisotropy, causing a component to be temperature insensitive. Nevertheless, the treatment temperature in these studies is as high as 600 °C ~ 1200 °C, which is far more than the temperature used in this work, so this can not explain these results. In addition, we also found that all the increases in inductance after bias tended to be of a specific value if the samples were subjected to a subzero temperature after cooling.

We separated the cycling of the TC profile into two parts, which were the treatment cycles and high-low temperature range, and treated the chip samples individually, and the results are shown in Table 3. When the number of cycles was less than 40, the increase in inductance would start to reduce significantly from 10 to 1 cycle, so the maximum increase in inductance appeared at 10 cycles or more, and this can also explain the low increase in inductance in Fig. 11, due to few treatment cycles. We limited the cycling temperature in the 125 °C ~ 25 °C and 270 °C ~ 25 °C ranges, and treated the samples for one cycle, and the results are shown in Table 3. Comparing the results for No.1 ~ No.5, it is clear that the very low increase in inductance increment of the 125 °C ~ 25 °C set was due to the very few cycles, however, the increase in inductance of the 270 °C ~ 25 °C set was as high as that was seen with the reflow treatment, even though the number of cycles was as the same as for the 125 °C ~ 25 °C set. We measured the inductance of these samples after bias, and the results are shown in Fig. 12.The 270 °C ~ 25 °C set showed a significant drop in inductance after bias, revealing that the increase in inductance after 270 °C ~

Table 3 The inductance shift of chip samples after thermal cycling treatment.

No.	Highest temp (^{o}C)	Lowest temp (^{o}C)	Cycle number	Inductance change (%)
1	125	-55	40	6.15
2	125	-55	20	6.37
3	125	-55	10	5.61
4	125	-55	2	4.37
5	125	-55	1	3.87
6	125	25	1	3.5
7	270	25	1	10.53

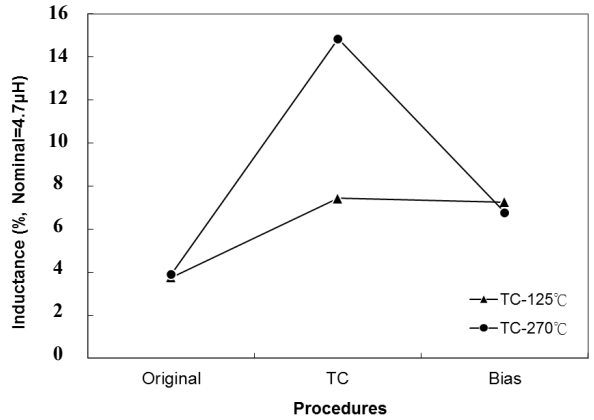


Fig. 12 The inductance shift of chip samples undergoing thermal cycling with different peak temperatures.

Table 4 The inductance shift of chip samples after the subzero temperature condition.

Highest temp (^{o}C)	Lowest temp (^{o}C)	Inductance change after treatment (A) (%)	Inductance change after bias (B) (%)	(A)+ (B)(%)
270	25	11	-8.5	2.5
270	-40	10.5	-5.03	5.47
125	-40	3.19	1.29	4.48
25	-40	1.67	3.24	4.91

Table 5 The inductance shift of chip samples after the test shown in Fig. 3.

Treatment	Inductance change rate after treatment (A) (%)	Inductance change rate after bias (B) (%)	(A) − (B) (%)
(a)	11	-8.5	2.5
(b)	10.5	-5.03	5.47
(c)	5.62	-5.21	0.41
(d)	6.77	-3.04	3.73

25 ^{o}C treatment came entirely from the peak temperature, which was over Curie point, and there was no contribution from the cycling itself. In addition, we also found that the increase in inductance seemed to move toward to a specific value after bias, even when the peak temperature of treatment was different for the various chip samples.

The TC profile contains the high temperature, cooling, cycling, and the subzero temperature. We loaded the samples at -40 ^{o}C, and the results are shown in Table 4. The results show that the subzero temperature seemed to inhibit the remanence. For the examples in Table 4, comparing the inductance levels after bias for the chip samples for which the treatment temperature was over the Curie point with and without subzero conditions, the inductance drop was reduced to 3% ~ 4% for the former. Column (A) + (B) in Table 4 shows the difference between the final and initial inductance levels, and from this data we can see that the experiment set without subzero treatment had only a 2.5% increase in inductance, while the other three sets had a 4.5% ~ 5.5% increase in inductance. This phenomenon is very similar to that was seen in Figs. 11 and 12; that is, if the sample is cooled rapidly to subzero temperature, the increase in inductance will move toward a specific value after bias. We synthesized the results of 270 ^{o}C of Fig. 11 and Tables 3 and 4, and then rearranged them into Fig. 13 and Table 5, and compared the data as-received. It can be seen that: (1) the increase in inductance of (a) and (b) is greater than that of (c) and (d), and this relates to the level of peak temperature; (2) the fall in inductance after bias of (b) and (d) is greater than that of (a) and (c), and this is related to the subzero temperature. Furthermore, we carried out the last experiment to distinguish the contribution of remanence and stress to the increased induction after thermal treatment of the chip samples, and the results are shown in Fig. 14. The 200 ^{o}C ~ -40 ^{o}C set and 250 ^{o}C ~ -40 ^{o}C set had different temperature ranges, and even though the differences in temperature were 240 ^{o}C and 290 ^{o}C, both had the same increase in inductance of 5%, and this result is still consistent with the phenomenon that we mention earlier. Nevertheless, comparing 250 ^{o}C ~

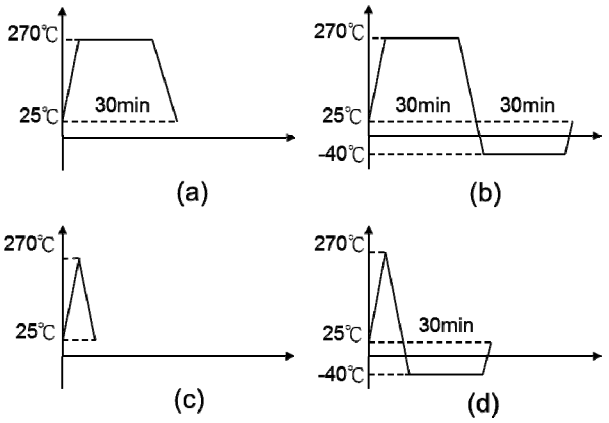


Fig. 13 The treatment profiles of chip samples to see the role of subzero temperature; (a) without the subzero temperature stage, (b) with the subzero temperature stage, (c) without soaking time at the peak temperature and without the subzero temperature stage, and (d) without soaking time at the peak temperature and with the subzero temperature stage.

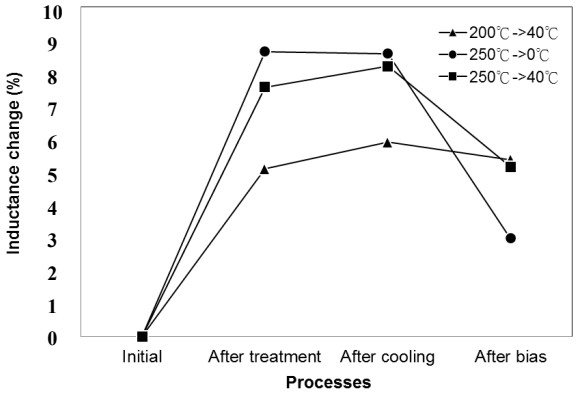


Fig. 14 Different treatment ranges of temperature for the chip samples.

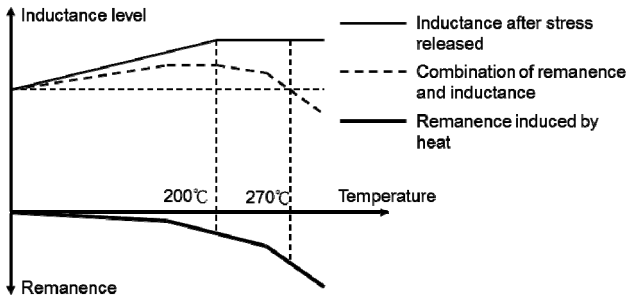


Fig. 15 The inductance change caused by the stress-release and remanence.

-40 °C and 250 °C ~ 0 °C, even though the later had 250 °C temperature difference, it only had 3% increase in inductance. According to the previous analysis, we can conjecture that, in this 5%, 2% was contributed by the remanence that was inhibited in the subzero temperature condition, and 3% was contributed by the stress, which was released in the cooling stage.

As we conjectured earlier, the release of stress is an irreversible change, and once stress has been released, all the change in inductance after thermal treatment comes from the change in magnetic status. The data in this work show that both stress release and change in magnetic status increase along with the temperature, and that the stress is completely released at around 200 °C, while the magnetic status continuously changes, and thus when the temperature reaches and exceeds 270 °C, the increased change in magnetic status counteracts the contribution of stress release, as seen in the significant fall in inductance. This process can be seen in Fig. 15. Furthermore, when the residual stress no longer exists inside the chip samples, this hindrance to the reaction between magnetic status and heat disappears, and thus the reaction is increased. Therefore, even if the chip samples have undergone the same conditions of treatment or bias, due to existence or absence of residual stress, or before or after thermal treatment for a single chip sample, the change in inductance will not be the same, and this can explain the results shown in Fig. 7.

We can draw the following conclusions based on these results.

(1) When the peak temperature of thermal treatment is higher, the increase in inductance after treatment is also higher, but this will then drop drastically thereafter when the bias is applied to the chip samples, and this shows that the increase is due to both stress release and remanence.

(2) If the temperature is cooled to below zero after thermal treatment, the fall in inductance will be reduced when the bias is applied to the chip samples, and this shows that the stress is released during the cooling stage and that remanence is inhibited by the subzero temperature.

(3) The higher the temperature, the greater the

increase in inductance. However, the level of residual stress is a constant value, that is, when the temperature is higher than a specific point that causes the contribution of magnetic status to be higher than that of stress, and then the inductance level will be even lower than the initial level when the bias is applied to the chip samples.

The results of this work show that the major difference of effect between the reflow and TC treatments is the inductance performance after bias and subzero temperature. However, the finding that the subzero temperature inhibits the remanence is inconsistent with the results of another study [12]. This earlier study used a sample that was circular and made of pure ferrite and wound coil. The chip samples we used were components with silver coil inside and there was cofiring of the silver coil and ferrite, and, based on the results of another study we carried out and as noted in the literature [9], not only the difference in shrinkage between the silver coil and ferrite, but also the diffusion and segregation of silver ions during sintering, all create much more complicated stress within a component compared to that was seen with a pure ferrite component. Moreover, after sintering, this complicated stress will remain and interact with the heat and magnetic field, and this causes a very different kind of inductance shift when the components are under thermal treatment or bias conditions.

4. Conclusions

In this work, we performed measurements of different combinations of thermal conditions and then compared the results. Based on the results, we can explain the components of inductance shift after different thermal treatments from the relationships among the temperature, stress and magnetization, and we also examined the contribution of each stage of the thermal profile to the inductance shift.

(1) To increase the temperature stability of inductance, preliminary thermal treatment to the chip inductors is necessary, and if the temperature of this is higher, then this will raise both the inductance and stability to temperature. However, the inductance will drop significantly after the bias condition, and this phenomenon only occurs with reflow treatment, but not with TC treatment, and the results of this work show that the cause of the increase in inductance includes both the release of stress and the change in magnetic status in the chip inductors.

(2) After analyzing the TC profile, the results show that the stress release occurs in the cooling stage, and the subsequent subzero temperature will inhibit the remanence induced by the reaction of the bias and magnetic status.

(3) In addition, the higher the temperature, the greater the increase in inductance. Nevertheless, the residual stress remains constant, so if the treatment temperature is higher than a specific point, the contribution of the change in magnetic status will counteract the contribution of stress release, and this will cause the inductance level to be even lower than the initial value after the treatment and bias.

(4) Comparing the manufacturing process and performance after thermal treatment of components made of pure ferrite with wound wire and multilayer chips, only the later has remanence, and this is because of the residual stress induced by cofiring of silver coils and ferrite inside the components, and the residual stress not only affects the inductance level directly, but also reaction between magnetic status and heat.

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